REMARKS

Claims 1 and 3-13 are pending.

Claims 8-10 are allowed, and independent claim 8 is amended to correct a typographical error introduced in the previous amendment.

Claims 1 and 11 are amended. Thus, pending claims remain for reconsideration, which is requested.

Claim Rejections Under 35 USC §103

On pages 2-5 of the Office Action the Examiner rejected claims 1, 3-7 and 11-13 under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] in view of U.S. Patent No. 6,266,779 issued to Kurd (hereinafter referred to as "Kurd"). The Applicants respectfully traverse the Examiner's rejections of these claims.

Claim 1 of the present application, as amended, recites "wherein ***the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state*** and ***the bus interface of the internal resource*** performs a bus management with the arithmetic unit ***in synchronization with the clock regardless of the state of the operation permission signal***." The Applicants respectfully submit that neither AAPA nor Kurd, taken alone or together, discloses or suggests at least this feature of claim 1.

Allowance of independent claims 1 and 11 is requested. The Office Action Response to Arguments (page 5) relies upon Kurd's FIG. 1 and column 3, lines 35-38 for allegedly discussing the claimed "a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock (m =< n), and supplies the operation permission signal to the internal circuit of the internal resource" and relies upon AAPA's discussion of a conventional microcontroller using a frequency divider 30 and a bus bridge 32 to allow for resources to operate at a clock different from the arithmetic unit's clock (e.g., CPU). However, while Kurd discusses accommodating components operating at different frequencies, Kurd's FIG. 1 and column 4, lines 1-16 fail to disclose expressly or implicitly any particular system configuration, namely the claimed "***an arithmetic unit operating in synchronization with the clock; an internal resource connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit both of which operate in synchronization with the clock ...***" In other words, Kurd is silent on the claimed "internal resource (FIG. 3, (12, 18))... having at least a bus interface (14, 20) and an

internal circuit (e.g., without limitation, 16, 22)," so Kurd cannot serve as any evidence to one skilled in the art to be combined with AAPA and even further modify the AAPA to provide the language of the claims, namely "internal circuit of the internal resource operates in synchronization with the clock when the operation permission signal denotes the operation permission state and the bus interface of the internal resource performs a bus management with the arithmetic unit in synchronization with the clock regardless of the state of the operation permission signal."

Therefore, a prima facie case of obviousness based upon AAPA and Kurd cannot be established, because there is no evidence expressly or implicitly to one skilled in the art to combine Kurd's generation of different sets of clock enables for each of a plurality of clock ratio signals, while being silent on any computer system configuration, with APPA's discussion of conventional microcontrollers, which use a frequency divider 30 and a bus bridge 32 to allow for resources to operate at a clock different from the arithmetic unit's clock (e.g., CPU), and then further modify AAPA and/or Kurd to provide the claimed "the ***internal circuit of the internal resource operates in synchronization with the clock*** when the operation permission signal denotes the operation permission state and the ***bus interface of the internal resource*** performs a bus management with the arithmetic unit ***in synchronization with the clock regardless of the state of the operation permission signal***," and seen the unexpected benefit that the claimed bus interface (14, 20) of the internal resource (12, 18) can perform bus management with a high speed clock because of the arithmetic unit's high speed clock, while the internal circuit (16, 22) of the internal resource (12, 18) can be controlled to slowly operate even though the internal resource's (12, 18) bus interface (14, 20) operates the arithmetic unit's higher clock speed. For example, the present application FIG. 3 and page 9, line 2 to page 10, line 21 support the claims. In other words, the language of the claims targets "***internal resource [FIG. 3, (12, 18)]… having at least a bus interface and an internal circuit***" and connected to an arithmetic unit (e.g., CPU), and the "***internal circuit of the internal resource operates in synchronization*** with the clock when the operation permission signal denotes the operation permission state and ***the bus interface of the internal resource [FIG. 3, (14, 20)] performs a bus management with the arithmetic unit in synchronization with the clock regardless of the state of the operation permission signal***." One unpredictable benefit in support of non-obviousness is the bus interface (14, 20) and the counter (16, 22) of the internal resource (12, 18) can cooperate at different clock frequencies.

Further, independent claim 11 requires the limitation "an operation permission signal having a lower frequency than the clock, and supplies the operation permission signal to the internal circuit of the internal resource," and requires the same limitation as independent claim 1, namely "wherein the internal circuit of the internal resource operates in synchronization with the clock when the operation permission signal denotes the operation permission state and the bus interface of the internal resource performs a bus management with the arithmetic unit in synchronization with the clock regardless of the state of the operation permission signal."

Allowance of independent claims 1 and 11 is requested, and further, dependent claims recite patentably distinguishing features of their own and/or are at least patentably distinguishing due to their dependencies from the independent claims.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,
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